

PATENT  
5732-00300/MA-069

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Verma et al.

Serial No. 10/080,036

Filed: February 19, 2002

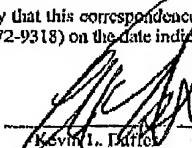
For: MEMORY MODULE HAVING  
INTERCONNECTED AND  
STACKED INTEGRATED CIRCUITS

Group Art Unit: 2827  
Examiner: L. Thai

Atty. Dkt. No. 5732-00300

I hereby certify that this correspondence is being transmitted  
via facsimile (703/872-9318) on the date indicated below:

3/25/03  
Date

  
Kevin L. Duffer

**RESPONSE TO OFFICE ACTION MAILED FEBRUARY 25, 2003** FAX RECEIVED

MAR 25 2003

Assistant Commissioner for Patents  
Washington, D.C. 20231

TECHNOLOGY CENTER 2800

Sir:

Responsive to the Office Action mailed February 25, 2003, please amend the captioned case as follows:

**IN THE CLAIMS**

Please cancel claims 21-31 without prejudice or disclaimer as to the subject matter recited therein. Applicants reserve the right file a divisional application capturing the subject matter recited in claims 21-31 canceled herein.

**REMARKS**

The present response cancels claims 21-31 in conformity with the following remarks. Claims 1-20 remain pending in the captioned case.